Examples of dry etching and plasma deposition at Glasgow University

Glasgow has pioneered and established many novel research activities involving the development of new dry etch processes and dry etch characterisation. As the absolute precision of pattern transfer and the process thermal budget are the dominant issues in the fabrication of nanometre scaled devices, our particular strength has been studies of plasma-induced damage and low-temperature plasma deposition for high-performance devices. These have lead to a fundamental understanding of the mechanisms of dry etching and have been of great relevance to device design and fabrication. The range of materials we etch is extensive and not only includes III-V, II-VI and IV semiconductors, but also high-k dielectrics, metals, insulators and plastics. JWNC etching and plasma deposition facilities are in constant use by members of a wide range of research groups within the university. We do collaborative research work with external organisations and a number of specific processes have been developed for industry.

Low-temperature PECVD for dielectric film deposition is one of the key processes in the fabrications of Si-Ge and III-Vs for high performance devices. Glasgow PECVD tools have been routinely used to deposit conformal and uniform dielectric films of SiO2, SiNx as well as low stress SiNx at ~300°C.

Glasgow has developed a novel room temperature ICP-CVD technology, which has yielded high-quality low stress SiN films with very low hydrogen content <3at.%. The film optical index is well correlated with the film composition. The main advantage of ICP-CVD over PECVD is its high-density plasmas. The optimised deposition conditions can counterbalance the negative effects of lowering deposition temperature. Ultra thin 5nm room-temperature-grown ICP-SiN film embedded in a MIM capacitor with 100% yield across a wafer was realised with a capacitance of 6.7fF/µm² and a breakdown
electric field $>3 \times 10^6 \text{Vcm}^{-1}$. Very little plasma-induced damage was observed on Van de Pauw samples of GaAs-based HEMT layer structures grown by MBE. The ICP-SiN has been successfully incorporated into Si-Ge and III-V fabrication processes.

We hope the following library of images highlights the breadth of experience we have in applying both dry etching and plasma deposition to micro and nanofabrication.

30 nm tungsten grating by RIE using SF$_6$

Ring resonator in GaAs/AlGas by RIE using SiCl$_4$

Photonic bandgap structure etched in SiCl$_4$
An array of pillars in gallium nitride formed by patterning and etching a silicon nitride mask using CHF₃ followed by gallium nitride etching using CH₄/H₂.
60 nm tungsten gates with resist mask still to be removed. Low damage W sputtering and RIE using SF₆/N₂ were used.

25 nm wide sputtered W gate formed by low damage RIE using SF₆/N₂, with room temperature ICP-CVD SiN side-wall spacers.

Liquid flow channels in silicon etched by STS-ICP using SF₆/C₄F₈.
15 µm wide Si trenches with very good anisotropy and very high aspect ratio etched by STS ICP using SF₆/C₄F₈ plasma.

40 nm wide Si wires with an aspect ratio of 13:1 etched by STS ICP using SF₆/C₄F₈ plasma.

On the left are sub 10 nm lines defined in diamond by RIE and O₂ using an HSQ mask which is still present. The diamond is etched to a depth of 20 nm. The etch tool used was an Oxford Plasma Technology BP80. On the right the HSQ mask has been removed using HF.
60 nm high aspect lines in GaAs by RIE using SiCl₄

Array of pillars in GaAs etched by RIE using SiCl₄

RIE low damage gate recess selective etching of GaAs on AlGaAs using SiCl₄/SiF₄/O₂

RIE CH₄/H₂ etching of InAlGaAs
High quality ICP-CVD SiN films with excellent conformal coating. The 50 nm SiN film has successfully covered a 150 nm metal step.

70 nm SiGe active device using the high quality low temperature ICP-CVD SiN. The distance to channel ~ 13nm.